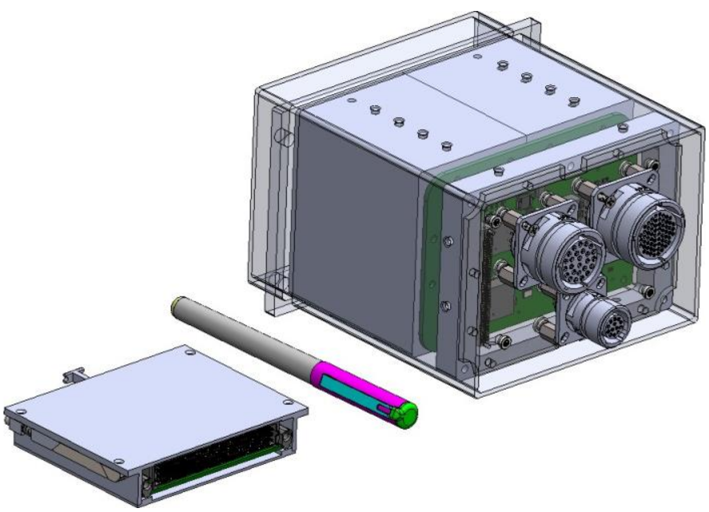
SFF and ALE-47 Programmer Modernization



The Open Group FACE® and SOSA® Consortia 2024 Technical Interchange Meeting (TIM), by:

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Case: AFLCMC/WNY 78ABW-2024-0099 CLEARED on 01 Aug 2024

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Executive Summary

The Open System Development Branch at the Georgia Tech Research Institute (GTRI) is working with the GTRI Warner Robbins Field Office to assist AFLCMC/WNY with an ALE-47 Programmer (PGMR) Technology Upgrade. The ALE-47 is a countermeasure dispenser system. The ALE-47 PGMR executes communication and control for the system. This development effort seeks to align the ALE-47 PGMR with USAF MOSA initiatives by incorporating SOSA® and HOST standards which enables multi-vendor, modular plug-in cards (PICs). This technical brief describes some of the major design decisions made by the GTRI team to apply the unfinalized VITA 90.x Small Form Factor (SFF) standards to a legacy avionics system upgrade. Included is an objective and requirements analysis, basic PIC connectivity overview, and description of the prototype.

This document aims to inform stakeholders of design considerations when implementing MOSA during legacy system upgrades.

GTRI VITA 90 Small Form Factor Prototyping: ALE-47 PGMR

The Open Systems Development Branch (OSDB) at GTRI has been working on a MOSA prototype for the ALE-47 PGMR in support of AFLCMC/WNY's ALE-47 Modernization effort. GTRI's OSDB directly supports development of MOSA standards and prototypes MOSA systems that align to open standards in efforts to advise on the published standards and to demonstrate advanced capabilities on MOSA systems. OSDB's MOSA SFF portfolio includes investigations and research into VITA 90 usage and applicability with DoD avionics programs. These programs have, so far, yielded a 9-slot development chassis and four (4) SFF PICs.

The request to build a SFF ALE-47 PGMR prototype is gratefully accepted and viewed as a pioneer usage for SFF/VITA 90 PICs in an important and widely used application. The ALE-47 PGMR Prototype program's objective is to create a hardware prototype that will function as a drop-in replacement for the legacy unit. A software port is not included in the effort so full software functionality will be implemented in a follow-on effort. The prototype will maintain the external dimensions and interfaces of the legacy unit and contain three (3) PIC slots for 19mm VITA 90 PICs. Some of the project deliverables include:

- PGMR Prototype Chassis

  Chassis includes a shell, framing, heatsinks and backplane with external M38999 connectors. The PGMR Prototype maintains all legacy connectors and adds an additional ethernet interface for future use (e.g. OMS/UCI).

- VITA 90 Single Board Computer (SBC)

  The SBC is a 19mm module with wedgelocks that is comprised of a 4-core ARM System on Module (SOM), a GTRI designed carrier card, and an enclosure.

- VITA 90.3 28VDC Power Supply Module (PSM)

  The PSM is a 19mm module with a custom PCB for converting 28VDC aircraft power into 12V/5V/3.3V power for PICs. This PSM includes some internal EMI protections.

- VITA 90 HOST Legacy I/O PIC

  The Legacy I/O PIC is a 19mm module that contains an FGPA to interface with discrete signals, RS422 signals, and MIL-STD-1553 data busses that are unique to the aircraft. This PIC contains a custom signal profile/pinout that is defined in HOST.

- ALE-47 Specific Verification and Validation Test Device

  This test device is specific to the ALE-47 PGMR and will exercise its I/O based and data busses to demonstrate functionality.

The Program will deliver end of Oct FY24. All the components listed above are GTRI designed and built under US Government Funding and resulting designs and outputs are property of AFLCMC/WNY.

Prototype Function and Purpose

The ALE-47 PGMR prototyping program serve two goals, 1) generate design guidelines, lessons learned, and requirements for the design and acquisition of a fieldable unit, and 2) create a representative system testbed for software development activities like porting legacy software and developing containerized software solutions. The PGMR prototype is a technology readiness level (TRL) 5-6 unit that proves out the feasibility of the SFF approach in a laboratory environment. The output of the current effort can then drive a TRL 7-8 development effort. The prototype configuration includes:

- Three SFF PICs for that accomplish PGMR functions
- 19mm SFF PICs with wedgelocks
- Omission of backplane ethernet between PICs
- Addition of ethernet to SBC PIC and Chassis Manager over M38999 rear panel connector

The PGMR uses three (3) unique slot profiles to accomplish its functions. Two (2) of the three (3) slot profiles appeared in SOSA Snapshot 3 and originated in VITA 90 draft standards. These are the 90.3 Balanced PSM profile and the 400 Pin SBC profile with overlay pins. The third profile is utilized by the Legacy I/O PIC and is not included in VITA 90 or SOSA Snapshot. Instead, this profile is captured within a HOST Tier 3 Specification and includes specific aircraft interfaces. The aircraft interfaces include signals such as 28VDC discretes, MIL-STD-1553 data busses, and RS422/485 interfaces. Integrators will often bring legacy interfaces into a custom PCB (sometimes co-located with a Chassis Manager) and/or XMC overlays on SBCs. While this approach is valid, utilization of HOST's Tier 3 specification process facilitates

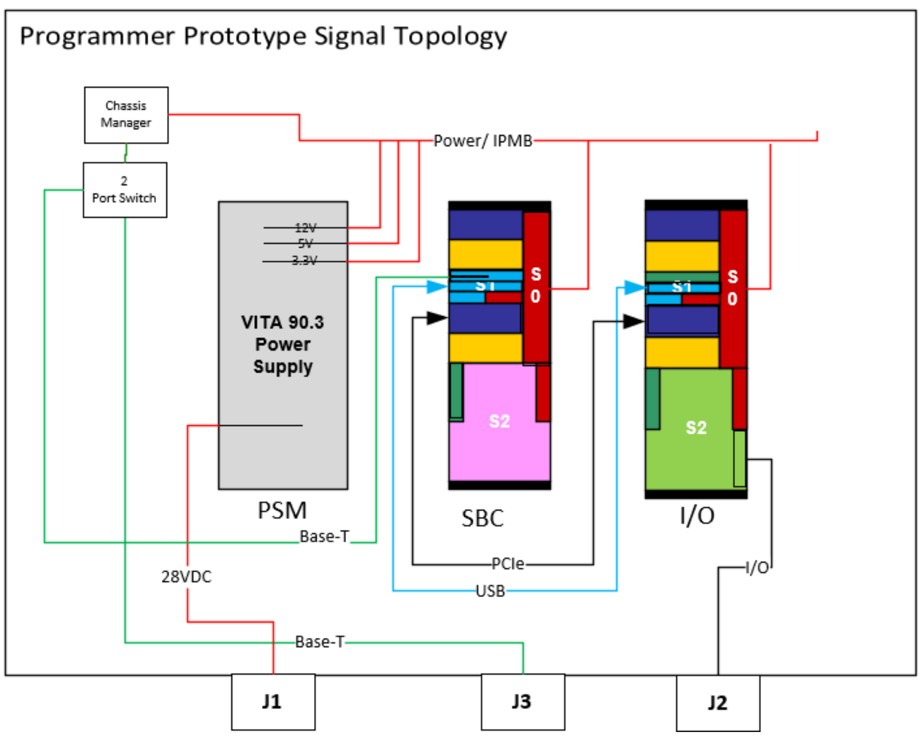

Figure 1: ALE47 PGMR Topology

definition of a custom profile overlay while still enabling a competitive acquisition strategy. It also modularizes all the active electronics within the unit into standard PIC form factors.

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SFF and ALE-47 PGMR Upgrade

Figure 1 outlines the basic signal connectivity between modules in the PGMR prototype. I/O and control interfaces are processed by an I/O PIC and communicated to the SBC via PCIe, essentially converting the legacy I/O signals into high-speed messages for the SBC's processor. The PSM PIC supplies a balanced voltage output with 12V/5V/3.3V rails and internal EMI filters.

To reduce the component count and SWaP of the PGMR prototype there is no backplane Ethernet utilized between the PICs. High-speed Ethernet adds cost and complexity to designs because it requires at least one Ethernet switch PIC and high-speed transceivers and technology stacks at each endpoint. The decision to not implement Ethernet within the PGMR was made because the PGMR interfaces are low-bandwidth and fast-response, and processing power must be kept low to meet SWaP requirements. Other systems may benefit from low-cost/low-SWaP strategies such as this since it doesn't prohibit integration of the unit with other systems and is allowable within the open standards. The high-speed backplane Ethernet interfaces were not routed on the PGMR prototype backplane either due to I/O routing density. OSDB will typically route all plugin slot profile signals on a backplane even if they are not utilized by certain PICs. This helps to future-proof systems and facilitates the incorporation of PICs that do utilize those interfaces in the future.

The only external addition to the PGMR prototype is the third rear panel connector which implements a single lane of 1GBEBASE-T Ethernet. This interface is intended for debug purposes and direct interfacing with the SBC PIC. However, it can also be utilized for future Command and Control functionality via a standard like OMS/UCI. This new interface is being called the "Avionics Expansion Bus" and is a rugged Series 3 D38999 connector.

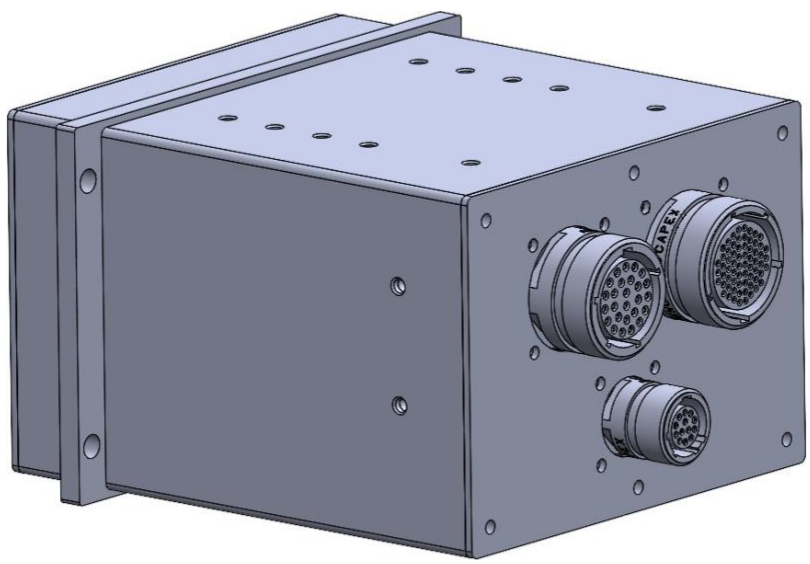

Figure 2: Rear of PGMR Prototype showing Avionics Expansion Bus connector

SFF and ALE-47 PGMR Upgrade

Prototype Construction

The ALE-47 PGMR prototype is comprised of 12 mechanical components and six (6) PCBs. Each PIC is enclosed by a two-piece enclosure as shown in Figure 4. The PICs slide into the heatsink and interface with a backplane. The backplane and the rear panel PCB are joined by an intermediary interface PCB that hosts the Chassis Manager circuits. A partially exploded view of the PGMR prototype is shown in Figure 3. The backplane (the leftmost PCB) is to the right of the mechanical heatsinks and the rear interface panel PCB can be seen just to the left of the circular connectors. There is a small on-board two-port Ethernet switch co-located with the Chassis Manager so that both the Chassis Manager and SBC are reachable via the Avionics Expansion Bus interface. For future development this interface will facilitate in-band System Management communications. The M38999 connectors interface with the rear panel PCB via PC tail contacts. Each PIC utilizes wedgelocks and a small handle for removal. Opening the front panel of the PGMR provides access to the PIC wedgelocks so that the PICs can be removed while the chassis remains installed in a system.

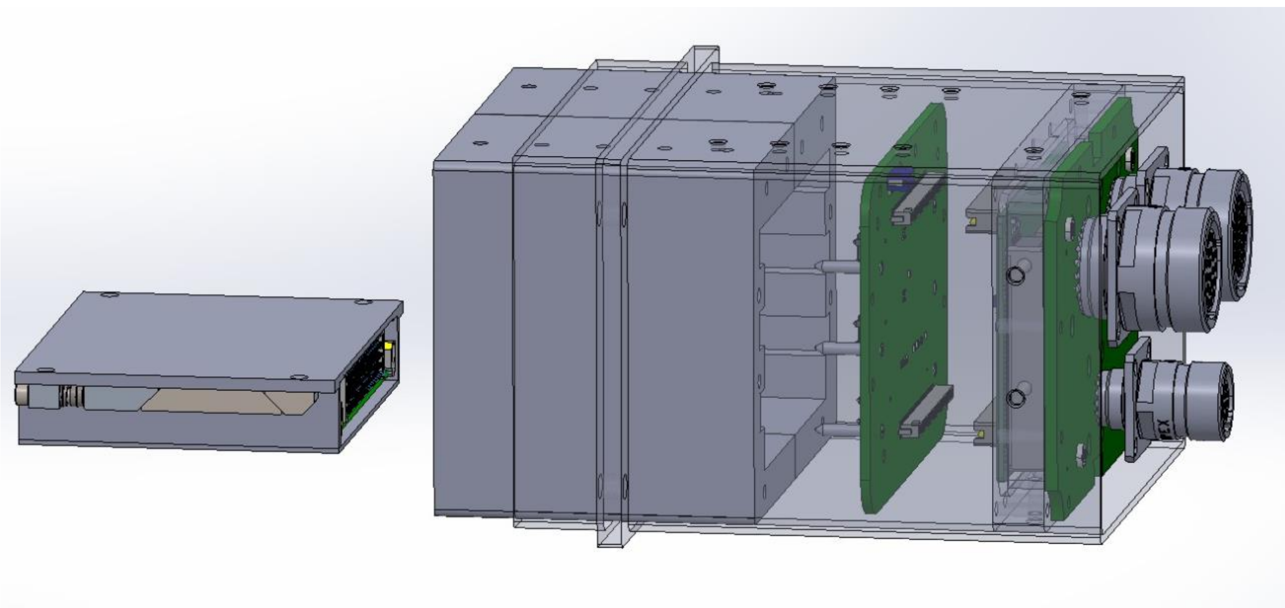

Figure 3: Semi-Exploded View of PGMR Prototype

The rear panel PCB interfaces with the backplane PCB via stacking connectors. These are non-ruggedized connectors which will need to be replaced with rugged connectors in a fieldable design. GTRI assumes a more-rugged solution for this interconnect such as flex PCBs will be used in a fieldable design. The PGMR chassis components are designed for low-quantity prototyping and quick manufacture. The heatsink tolerancing, potential fabrication method recommendations, and thermal simulations will be a primary output from this mechanical design exercise. The prototype chassis consists of EDM cut, multi-axis machining and metal sintering methods. A fieldable system could center around machined and extruded components that are brazed together for 1-piece construction if desired.

VITA 90 SFF PICs are attractive for cockpit-mounted and SWaP-constrained avionics systems. The ALE-47 PGMR is designed for DZUS common avionics rail mounting. The ability to mount SFF systems in locations that are unavailable when using other open standards is a great advantage, but it also comes with limitations.

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SFF and ALE-47 PGMR Upgrade

These SWaP-limited spaces have lower airflow, cooling, and power draw capabilities when compared to spaces that can accommodate large radars or other avionics. Implementing high-performance applications on SFF PICs may prove challenging due to the cooling and power requirements needed to make those high-performance capabilities a reality. This is why OSDB is first targeting a basic PGMR upgrade where low-SWaP technologies like an ARM processor still have ample processing resources to perform the legacy processor's functions while staying within the legacy SWaP constraints. After this initial upgrade is successful additional capabilities can be implemented with the remaining processing resources. The PGMR prototype will be capable of operating its processor at roughly 3x the current processing speed needed for just the legacy application. The PGMR prototype also has expandable memory. To hard-limit the power draw of the entire unit the prototype can current limit the PSU PIC via software commands. These features ensure that the PGMR prototype can operate as a drop-in replacement for a legacy unit while still being upgradable with minimal investments in the future: once the legacy functions are fully ported and the software is load tested, additional applications can be implemented with any remaining power capacity available to the PGMR.

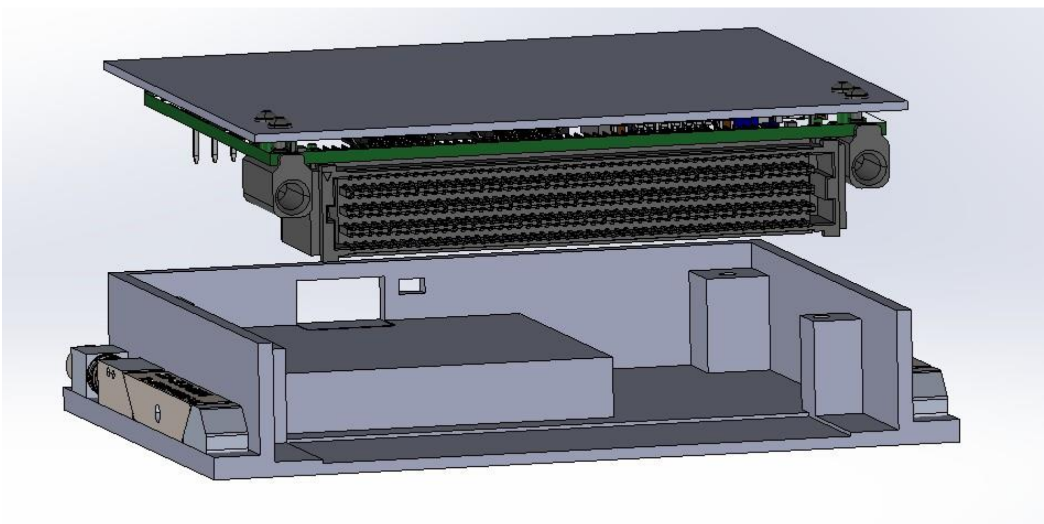

Figure 4: VITA 90 Modules 2 Piece Enclosure

Conclusion

MOSA-designed systems facilitate modularity, interoperability, and upgradability not previously possible in avionics systems. This also facilitates faster capability integration and deployment. Jumping into MOSA-based design can be a daunting task that requires skilled engineers and managers well-versed in many aspects of technology. OSDB at GTRI recognizes this difficulty and produces content, like this technical brief, to elucidate the technical hurdles and bring forward innovative solutions for stakeholders and MOSA consortium members a whole. The ALE-47 PGMR prototype and associated deliverables discussed here will be appropriately summarized and distributed at the program offices discretion for the benefit of SOSA Consortium Members.

Referenced Documents

C212 Technical Standard for SOSA® Reference Architecture, Edition 1.0 (C212), published by The Open Group, September 2021; refer to: www.opengroup.org/library/c212

C220 Draft of VITA 90 VNX+ Base Standard, Rev 0.0, March 2024; refer to https://www.vita.com/StandardsUpdates

C410 Hardware Open System Technologies (HOST), V5 (HOST00001-12), created by GTRI for NAVIAR PMA209; refer to https://host-oa.com/

About the Author

Rafael Garcia is a Research Engineer in the Open Systems Development Branch at Georgia Tech Research Institute. He has several years of experience working with MOSA systems, mainly focusing on legacy avionics replacements and prototyping with emphasis on 3U VPX and SFF systems.

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The Open Group Future Airborne Capability Environment® Consortium or FACE® Consortium, was formed as a government and industry partnership to define an open avionics environment for all military airborne platform types. Today, it is an aviation-focused professional group made up of industry suppliers, customers, academia, and users. The FACE Consortium provides a vendor-neutral forum for industry and government to work together to develop and consolidate the open standards, best practices, guidance documents, and business strategy necessary for acquisition of affordable software systems that promote innovation and rapid integration of portable capabilities across global defense programs.

Further information on the FACE Consortium is available at www.opengroup.org/face.

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